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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/880,223	06/13/2001	Louis L. Hsu	728-208(YOR9-2001-0270 US	5309

7590 02/12/2004

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EXAMINER

RAO, SHRINIVAS H

ART UNIT	PAPER NUMBER
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2814

DATE MAILED: 02/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/880,223

Applicant(s)

HSU ET AL.

Examiner

Steven H. Rao

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 12 and 14-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☐ Claim(s) 12 and 14-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Priority

Receipt is acknowledged of paper submitted under 37 C.F.R. 114, claiming priority from U.S Serial No. 09/880,223 filed June 13, 2001 which papers have been placed of record in the file.

Request for Continued Examination

The request filed on 11/14/2003 for a Request for Continued Examination Application (RCE) under 37 CFR 1. 114 based on parent Application No. 09/880,223 is acceptable and a RCE has been established. An action on the RCE follows.

Preliminary Amendment Status

Acknowledgment is made of entry of preliminary amendment filed 08/ 07/ .2003 as requested in 1 a. (ii) of the RCE transmittal.

Acknowledgment is also made of the Supplemental amendment faxed to Ex. Rao after 5.00p.m. on Friday Jan. 23, 2004 .

Therefore claims 12 and amendment and claims 14-16 as previously recited are currently pending in the Application.

Claims 1-11, 13 and 18- 30 have been cancelled by the preliminary amendment .

Claim 31 has been cancelled by the Supplemental amendment of 1/23/2004.

Specification

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 12-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 12 recites , " said transfer gate including a source/drain and body formed in a polysilicon layer" renders the claim indefinite because it is well known that the gate is separate stand alone part of the TFT and it is the TFT that includes the source/drain and the body .

Claims 14-17 are rejected at least for depending upon rejected claim 12.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

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invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 12 and 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,448,586 to Nemati et al. (herein after Nemati) in view of Kumagi (U.S. Patent .No. 5,357,125 herein after Kumagi) both previously applied . For response to Applicants' arguments see section below.

With respect to claim 12, a T-Ram array including a plurality of T-Ram cells arranged in an array (Nemati fig. 8, col. 6 lines 65-66), wherein each of the plurality of T-Ram cells includes a buried vertical thyristor region beneath at least a portion of a transfer gate region. (Nemati fig.8, p portion of 40 a, b, and c under respective gate 48).

Nemati does not label his gate as a transfer gate however it is inherent from the description in col. 7 lines 1-15 that Nemati's gate 48 functions like a pseudo TFT (similar to applicant's description at page 5 of the specification) and therefore one of ordinary skill in the art would readily recognize Nemati's gate 48 to be a transfer gate similar to that claimed.

The remaining limitations of claim 12 are :

And a horizontally stacked pseudo-TFT transfer gate , (see above) , said transfer gate (i.e. pseudo TFT) including a source/drain and body formed in a poly silicon layer . (Nemati col. 5 lines 46 to 61) .

Assuming arguendo that the newly added limitation, " wherein said thyristor being buried underneath said transfer gate, wherein said transfer gate covers the entire top surface of said first device, and further wherein the top surface of said transfer gate

forms a planar top surface of each said transfer gate of each of said T-Ram cell." is supported by the specification as originally filed the following rejection is made.

Nemati does not specifically describe the newly added limitation wherein said second device being buried underneath said second device, wherein said second device covers the entire top surface of said first device, and further wherein the top surface of said transfer gate forms a planar top surface of each said transfer gate of each of said T-Ram cell.

However, Kumagi in figures 1-5 and col. 5 lines 61-68 and figures 2 and 5 describes wherein said second device being buried underneath said second device, wherein said transfer gate covers the entire top surface of said thyristor, and further wherein the top surface of the transfer gate forms a co-planar top surface of each said transfer gate of each of said T-Ram cell to form a semiconductor device that is readily integrated into one chip and can be effectively used as a power switching device.

Therefore it would have been obvious to one of ordinary skill in the art to include Kumagi's said thyristor buried underneath said transfer gate, wherein said transfer gate covers the entire top surface of said thyristor, and further wherein the top surface of the transfer gate forms a co-planar top surface of each said transfer gate of each of said T-Ram cell and wherein Nemati's device to form a semiconductor device that is readily integrated into one chip and can be effectively used as a power switching device.

With respect to claim 14, wherein each of the plurality of cells has a size less than or equal to $8F^2$. (It is well known in the prior art that T-ram cells have a size of $8F^2$ or less as admitted by the applicants' herein in their co-pending application No.2002/0093030 published on July 18, 2002 in its abstract lines 10 –13 etc.)

With respect to claim 15, wherein said substrate is a semiconductor SOI or bulk wafer (Neamti fig. 6a # col. 6 lines 20-27).

With respect to claim 16, wherein the base of said thyristor is surrounded by a surround gate . (Nematı fig. 8 thyristors 40 a, b and c being surrounded by the gate 48).

With respect to claim 17, Nematı describes wherein each of the plurality of T-Ram cells includes structure for the traversal of at least two word lines there through. (Nematı fig. 5, col. 5 lines 33-60) said planar top surface of each T-Ram cell provides for simplified fabrication of metal wirings, said wirings being fabricated over said planar top surface of said T-Ram cells, said wirings for inter connecting said T-Ram cells .

The limitation , "said planar top surface of each T-Ram cell provides for fabrication of metal wirings, said wirings being fabricated over said planar top surface of said T-Ram cells, said wirings for inter connecting said T-Ram cells " is taken to be a product by process limitation.

Response to Arguments

Applicant's arguments filed 08/11/2003 and 1/23/2004 have been fully considered but they are not persuasive for the following reasons:

Applicants' arguments of 8/11/ 2003 namely, " In contrast, it is inherent in a pseudo_TFT gate as recited in claim 12 as amended that both the source/ drain and the body are contained in a polysilicon layer. " was not persuasive because the same was not recited in the claim 12 till applicants' amendment of 1/23/ 2004, and therefore Applicants' arguments were not commensurate in scope with their arguments .

Applicants' amendment of 1/23/2004 again has 112 problems because claim 12 presently recites " said transfer gate including a source/drain and body formed in a polysilicon layer ". It is understood by one skilled in the art that a gate does not include a source/drain and body regions , but that a pseudo-TFT may include the source/drain and body regions, assuming this is what Applicants' meant , all the added limitations are taught by Nemati col. 5 lines 46 to 61.

Applicants' next contention that Nemati teaches away from the invention claimed in claim 12 because Nemati has a metallization layer over the surface of the thyristor , which is where the horizontally stacked pseudo- TFT transfer gate is located is not persuasive firstly this limitation is currently recited in claim 12.

Assuming arguendo that Applicants' recite this limitation, Applicants' above contention is still not persuasive because Nemati's structure is similar at least to Applicants' structure described in figure 13, wherein a conductive layer 108 (n+) is on the top surface of its thyristor (similar to Nemati's metallization layer) and the horizontally stacked pseudo-TFT is present above the conductive layer 108.

Therefore Nemati does not teach away from the invention.

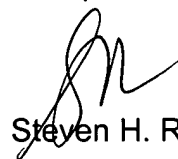
Applicants' next contention with respect to claim 17 that Nemati does not disclose word lines fabricated on a planar top surface is directly contrary to Nemati's teachings in figures 3a, b and 5 and col. 5 lines 28-50.

Dependent claims 14-16 and (17) were alleged to be allowable as they depend upon allegedly allowable claim 12.

However as shown above claim 12 is not allowable. Therefore claims 14-17 as also not allowable.

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Steven H. Rao whose telephone number is (571) 272-1718. The examiner can normally be reached on Monday- Friday from approximately 8:00 a.m. to 5:30 p.m.

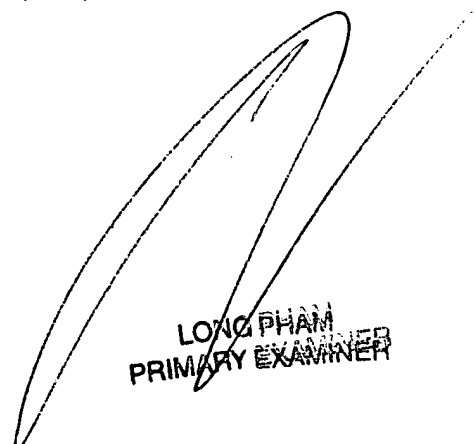
Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. The Group facsimile number is (703) 308-7724.



Steven H. Rao

Patent Examiner

January 21, 2004.



LONG PHAM
PRIMARY EXAMINER